REMARKS

I. CLAIM STATUS

Claims 1-34 remain pending.

II. REJECTIONS UNDER 35 U.S.C. § 103

Claims 1-3, 13-15 and 24-26 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Shen et al. (U.S. Pub. No. 2004/0093467) in view of Beardsley et al. (U.S. Pat. No. 6,425,050). Claims 4-12, 16-23 and 27-34 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Shen et al. in view of Beardsley et al. and further in view of Temple (U.S. Pat. No. 5,937,199). Applicants respectfully traverse these rejections because the cited art fails to teach or suggest each limitation of the claims, as is required for a rejection of this type. *See* MPEP § 2142.

For example, independent claim 1 recites in part: "wherein said Owner processor may displace the exclusive copy of said memory block, *and return said displaced copy of said memory block to said Home processor with a signal* indicating that said Owner processor remains a sharer of said memory block." Regarding this limitation, the examiner particularly cites Beardsley's Figs. 3 & 4; col. 5, lines 43-67; and col. 6, lines 18-33. Beardsley's Fig. 3 and col. 5 relate to the granting of cache access to destage track data back to a storage device from the cache.

As set forth in Figure 3, Beardsley discloses the following steps for destaging tracks from the cache device to the storage device: (1) check to see if another process has exclusive or semi-exclusive access to the track, prohibiting access by other users 102; if not (2) check to see whether the track is currently subject to a destage operation 106; if not, (3) check to see if the active writer count, i.e., number of writers accessing the track, is zero 108; if yes, (4) grant semi-exclusive access to the track 110, set the destage in progress flag 112, and increment the active users count 114. All the recited steps are meant to ensure that the tracks are not destaged from the cache to the memory until all users of the track have completed their tasks. Beardsley is completely silent as to any

signals from a user indicating that the user is still using a particular track, after that track has been destaged from the cache to the main memory. Therefore, Beardsley fails to disclose an Owner processor, i.e., a processor that was using a copy of the memory block in its cache, who "*return*[s] *said displaced copy of said memory block to said Home processor with a signal* indicating that said Owner processor remains a sharer of said memory block" as claimed in independent claim 1.

Beardsley's Fig. 4 and col. 6 relate to the granting of access to the tracks in the cache after the destaging has begun by downgrading the destage access from semi-exclusive to share access. However, Beardsley clearly teaches that such shared read access is not allowed *unless the data has not yet been displaced from the cache*. *See* Beardsley col. 6, lines 34-42 ("[A]ccess is not released if the entire track is not in cache, otherwise a new read request could request data records that are not in cache"). Therefore, Beardsley merely discloses a system whereby a track which was to be destaged from the cache to the memory storage will be retained on the cache if a new read request comes in for that track and the full track is still available in the cache. Col. 6, lines 18-30. Nowhere in col. 6 does Beardsley disclose a system where the memory block is returned from the cache to the memory storage together with a signal from the user/processor using that block in the cache before its return indicating that the user "remains a sharer" of said memory block.

The cited art thus fails to teach or suggest returning a signal to a home processor indicating that a remote processor, having displaced a memory block, remains a sharer of the block as required by the claim. Independent claim 1 and its dependent claims 2-12 are allowable for at least this reason.

Independent claim 13 recites in part "displacing said copy of said memory block from said cache memory ... [and] transmitting a message to said Home processor ... indicating that said Owner processor should still be deemed a sharer of said memory block." As noted above, the examiner particularly cites Beardsley, but Beardsley clearly teaches that shared access to data being destaged is allowed only if the data has not yet been displaced from the cache

and is wholly silent as to the possibility of sharing data by users after the data has been destaged from the cache to the memory storage. For at least this reason, the cited art fails to teach or suggest allowing a processor to be identified as a sharer after displacing the memory block from its cache. Independent claim 13 and its dependent claims 14-23 are allowable for at least this reason.

Independent claim 24 recites in part "said second processor may displace the exclusive copy of said memory block [and transmit] a signal to said first processor indicating that said second processor ... should remain a sharer of said memory block." As noted above, the examiner particularly cites Beardsley, but Beardsley clearly teaches that shared access to data being destaged is allowed only if the data has not yet been displaced from the cache. Col. 6, lines 25-27 ("The storage controller 8 determines whether the full track flag 22 is set. If not, then request to change the access to shared is denied."). For at least this reason, the cited art fails to teach or suggest allowing a processor to be identified as a sharer after displacing the memory block from its cache. Independent claim 24 and its dependent claims 25-34 are allowable for at least this reason.

III. CONCLUSION

In the course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the cited art which have yet to be raised, but which may be raised in the future.

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are

hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,

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